PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Kuzemchak et al. (TI-32964) Conf. No. 7240

Serial No. 10/022,972 Group Art Unit: 2192

Filed: December 13, 2001 Examiner: Chow

For: Method for Enhancing the Visibility of Effective Address Computation in Pipelined Architectures

SECOND SUBSTITUTE APPELLANTS' BRIEF

Commissioner for Patents
Washington, DC 20231

Dear Sir:

Appellants respectfully present their brief in support of their appeal of the final rejection of claims in this case. The Notice of Appeal was filed on July 18, 2005, as indicated on the date stamped on the return postcard from the Patent and Trademark Office. This Substitute Appellant's Brief is presented in response to the Notice of Non-Compliant Appeal Brief mailed May 16, 2006.

Real Party in Interest

The real party in interest in this application is Texas Instruments Incorporated.

Related Appeals and Interferences

Related copending application S.N. 10/017,777 is currently on appeal. Its claim 10 includes, *inter alia*, method steps similar to those in claim 1 of this application. This claim 10 is under final rejection, and is on appeal.

Status of the Claims

Claims 1 and 2 were finally rejected in the Office Action of April 19, 2005, and are the subject of the present appeal.

Status of Amendments

No amendment was presented after the final rejection. The claims on appeal in this case are therefore identical with those finally rejected.

A Terminal Disclaimer is filed in this application contemporaneously with this Appellants' Brief, relative to copending related application S.N. 10/017,077, to remove obviousness-type double patenting as one of the grounds of rejection in this application.

Summary of the Claimed Subject Matter

The claimed subject matter is directed to a method of determining, in software, the effective address of program instructions executed by a processor with a pipelined architecture. In the execution of a first program, the inventive method includes the calculating of an effective address delay of an instruction in the pipeline.[1] The specification discloses an example of this calculating operation as determining the number of CPU clock cycles from the entry of the instruction in the pipeline to the point in the pipeline at which effective address used in that instruction is fully computed, less the number of clock cycles that have elapsed since that instruction entered the pipeline.[2] Based on the result of this calculating, the claimed method determines whether a valid effective address for that instruction is available,[3] such as if the

[1] Specification of S.N. 10/022,972, process702 of Figure 7.
[2] Specification, *supra*, page 18, lines 7 through 11.
[3] Specification, *supra*, decisions 704, 706 of Figure 7.

effective address delay is zero.[4] If a valid effective address is not available,[5] the method computes an effective address and reports that effective address.[6]

The specification points out numerous important advantages of the claimed subject matter,[7] particularly in providing important visibility into effective addresses of instructions during software verification of pipelined processors, even in situations in which the effective address is altered during execution. As a result, the claimed method facilitates the portability of software routines from one processor architecture to another, even in situations in which the target architecture is a complex pipelined architecture.[8]

In response to the Notice of Non-Compliant Appeal Brief of February 22, 2006, Appellants respectfully submit that claims 1 and 2 on appeal do not include any step-plus-function elements.[9] As such, no additional identification regarding the structure, material, or acts described in the specification as corresponding to each claimed function is presented.[10]

Grounds of Rejection to Be Reviewed On Appeal

The rejection of claim 1

Claim 1 was finally rejected under §103 as unpatentable over the Laurenti et al. patent[11] in view of the Guerra et al. reference[12]. The Examiner asserted that the Laurenti et al. patent discloses determining effective addresses of instructions in a program executed on a pipelined

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[4] Specification, *supra,* page 18, lines16 and 17.
[5] Specification, *supra,,* decision 706.
[6] Specification, *supra,* page 18, line 23 through page 19, line 2, relative to decisions 708, 710 and process 712 of Figure 7.
[7] Specification, *supra,* page 16, line 14 through page 17, line 18.
[8] Specification, *supra,* page 16, line 14 through page 17, line 18, page 1, line 27 through page 2, line 8, and page 21, lines 15 through 25.
[9] 35 U.S.C. §112, ¶6.
[10] 37 C.F.R. §41.67 (c)(1)(v).
[11] U.S. Patent No. 6,658,578 B1, issued December 2, 2003 to Laurenti et al., and commonly assigned with this application. The European counterpart of this patent was published on April 12, 2000, as European Patent Application Publication No. EP 0992 916 A1, and as such the contents of the European counterpart are available as prior art under §102(b) and §103.
[12] Guerra et al., "Cycle and Phase Accurate DSP Modeling and Integration for HW/SW Co-Verification", *ACM* (June, 1999), pp. 964-69.

architecture with no external visibility into the pipeline, but did not disclose the specific steps of the claim.[13] The Examiner asserted that the Guerra et al. reference teaches those features, specifically "the capability to determine, calculate, compute, and report of instruction delay" as required by claim 1.[14] The Examiner further asserted that one skilled in the art would have obviously combined the teachings of Guerra et al. into the Laurenti et al. disclosure to model and integrate pipelined architecture, as motivated by the abstract of Guerra et al.[15]

Claim 1 (and claim 2) were also provisionally rejected under the doctrine of double patenting of the obviousness type, relative to copending commonly assigned application S.N. 10/017,077. As noted above, a Terminal Disclaimer relative to that copending application is now being submitted in this application, obviating the provisional double patenting rejection.

The rejection of claim 2

Claim 2 was finally rejected under §103 as unpatentable over the Laurenti et al. patent and the Guerra et al. reference as applied against claim 1, discussed above. The specific limitations of claim 2 were asserted as found in the Guerra et al. reference, including the "clock cycles calculation feature".[16]

Argument

It is axiomatic, in the patent law, that a *prima facie* obviousness determination of patent claims requires teachings from the prior art itself to appear to have suggested the claimed subject matter to a person of ordinary skill in the art.[17] If the Examiner fails to establish such a *prima facie* case, the obviousness rejection is improper and should be overturned on appeal.[18] In this regard, the *prima facie* obviousness determination requires a finding that all of the claim

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[13] Office Action of April 19, 2005, pages 9 and 10.
[14] *Id.*
[15] *Id.*
[16] Office Action, *supra*, page 11.
[17] *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993).
[18] *Rijckaert, supra.*

limitations are taught or suggested by the prior art.[19] If the suggestion or motivation to combine references is not supported by evidence, the combination is therefore simply an improper use of the inventor's own teachings in hindsight.[20]

Claim 1

Appellant respectfully submits that the Examiner has failed to establish a *prima facie* case of obviousness relative to claim 1, because the combined teachings of the applied references fall short of the requirements of the claim. Appellants therefore submit that the final rejection in this case is in error and should be reversed.

Accepting for the sake of argument that the Laurenti et al. patent teaches the elements of the preamble, Appellants agree with the Examiner that it fails to disclose the specific steps of the method.[21] But Appellants submit that the recited steps of claim 1 are also not disclosed by the Guerra et al. reference.

The Examiner asserts that the cited location of the Guerra et al. reference[22] teaches the "capability to determine, calculate, compute, and report of instruction delay as claimed".[23] Appellants disagree. Rather, this portion of the reference discloses that, in the event of an interrupt occurring with a conditional branch in the instruction fetch pipeline stage, the interrupt is delayed by one instruction cycle so that a "delay slot" instruction is executed before the interrupt is serviced, permitting the target address of the branch to be used as the return address from the interrupt routine.[24] The reference in no way teaches the calculating of any effective address delay of an instruction, nor the determining of whether a valid effective address for that instruction is available based on that effective address delay, nor the computing of an effective

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[19] *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974); *see also* Manual of Patent Examining Procedure, §2143.03.

[20] *In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ3d 1614 (Fed. Cir. 1999) ("Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability -- the essence of hindsight.").

[21] *See* Office Action, *supra*, page 10.

[22] Guerra et al., *supra*, page 966, right-hand column, and Figures 2 and 3.

[23] Office Action, *supra*, page 10.

[24] Guerra et al., *supra*, page 966, right-hand column, last paragraph.

address if a valid effective address is not available, all such steps required by claim 1. Indeed, contrary to the assertion by the Examiner,[25] the Guerra et al. reference does not perform any action relative to an "instruction delay"; the reference instead teaches the executing of a "delay instruction". The two are not synonymous.

Therefore, coupled with the Examiner's admission that the Laurenti et al. reference fails to teach the steps of claim 1, Appellants respectfully submit that the combined teachings of the applied references fall short of the requirements of claim 1.

Appellants also respectfully challenge the basis of the final rejection by way of which the teachings of the Laurenti et al. and Guerra et al. reference were combined. The Examiner asserted that the motivation to combine the teachings of these references was "to supplement Laurenti's disclosure of the pipelined architecture by the statistical traces taught by Guerra for the purpose of modeling and integration of pipelined architecture".[26] But the Guerra et al. reference does not teach anything about "statistical traces", especially in its cited location, which only teaches the executing of a "delay slot instruction" so that the branch target address is the return address from the interrupt. Nor do such "statistical traces", even if taught, have anything whatsoever to do with the method of claim 1. Accordingly, Appellants submit that the stated motivation for combining the teachings of the applied references would not lead one skilled in the art to practice the method of claim 1.

Further, Appellants submit that there is no sensible way to combine the cited teachings of the references in such a manner that is relevant to the claimed invention. The cited portion of the Laurenti et al. reference relating to an "effective address"[27] merely teach that, for a "long word data type" (*i.e.,* where the data value extends over two 16-bit words[28]), the address of the most significant word (MSW) of this long-word is either at the next lower address or the next higher address depending on whether the storage address is even or odd, respectively.[29] The cited

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[25] Office Action, *supra,* page 10.
[26] *Id.*
[27] Laurenti et al., *supra,* column 28, lines 15 through 27.
[28] Laurenti et al., *supra,* column 27, Table 10.
[29] Laurenti et al., *supra,* column 28, lines 15 through 27.

portion of the Guerra et al. reference directed to the "delay slot instruction" merely teaches the executing of a delay slot instruction of a conditional branch in response to an interrupt, so that the target address of that branch becomes the return address from the interrupt routine. It is far from clear *how* one skilled in the art might combine these Guerra et al. teachings regarding interrupt handling with the Laurenti et al. teachings regarding the address of the MSW of a long word data type, and it is farther yet from clear *why* one might make that combination. And even if one could imagine such a combination, it is beyond imagination that such a combination would result in the method of claim 1.

Appellants presented argument[30] after the final rejection along these lines, to which the Examiner responded. In that response, the Examiner asserted that the "delay slot" of the cited portion of the Guerra et al. reference "implies that a calculating/determining/computing and reporting has been done for the effective addresses of the instructions (otherwise how can this result been [sic] produced?)".[31] Apparently, therefore, the Examiner agrees with Appellants that the Guerra et al. reference does not expressly teach the steps of claim 1, but the Examiner now maintains that those steps are implicit in the reference. Appellants respectfully disagree with this characterization of the reference, again by wondering how the method steps of claim 1 are implicit in the reference. For example, exactly what is the "effective address" of an instruction in the Guerra et al. pipeline (certainly it cannot mean the same thing as in the Laurenti et al. reference, considering that there are no "long word" data types evident in the Guerra et al. reference)? What is an "effective address delay" according to the Guerra et al. teachings, and how is it necessarily calculated? And how does the Guerra et al. reference necessarily determine whether a valid effective address is available based on the current effective address delay, or implicitly compute that effective address responsive to determining that a valid effective address is not available? There is clearly no answer to any of these questions, because the Guerra et al. reference provides no teachings in this regard.

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[30] Request for Reconsideration filed July 18, 2005.

[31] Advisory Action of August 5, 2005, continuation sheet.

Because the combined teachings of the Laurenti et al. and Guerra et al. references fall short of the requirements of claim 1 and because the final rejection is not based on any other suggestion to modify those teachings so as to reach the claim, Appellants submit that a *prima facie* case of obviousness has not been made relative to claim 1.[32] Appellants further submit that because evidence to combine and modify these references so as to reach claim 1 is wholly lacking in this case, the alleged combination upon which the final rejection is based is therefore necessarily an improper use of Appellants' own teachings in hindsight.[33]

Appellants therefore submit that the final rejection of claim 1 is in error and should be reversed.

Claim 2

Claim 2 further specifies, relative to claim 1 upon which it depends, the manner in which the calculating step is performed, namely by subtracting the number of clock cycles that have occurred since the instruction entered the pipeline from the number of clock cycles required to compute the effective address of the instruction. Claim 2 further recites that the computing step is executed responsive to the current effective address delay being less than zero.

For the same reasons as discussed above relative to claim 1, Appellants respectfully submit that the final rejection of claim 2 is also in error and should be reversed.

Appellants further respectfully submit that the rejection of claim 2 is in error because the specific limitations of claim 2 were not found by the Examiner to be disclosed or suggested by the prior art, nor are such limitations present in the art.

The final rejection of claim 2 is based on a finding, by the Examiner, that the Guerra et al. reference teaches:

> The co-verification model consists of the ISA simulator and a Bus Interface Model, BIM (Figure 1a). The interface model itself is also partitioned into two

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[32] *See Royka, supra.*
[33] *Dembiczak, supra.*

> parts, the bus pin model and the bus cycle scheduler. The latter collects the information about the software events, identifies the corresponding hardware events, and schedules them in proper order for each clock cycle.[34]

The Examiner found that this passage specifies the "clock cycles calculation feature".[35] Appellants respectfully submit that this passage of the reference, and indeed the reference in its entirety, nowhere discloses or suggests the calculating of a current effective address delay by subtracting the number of clock cycles that have occurred since the instruction entered the pipeline from the number of clock cycles required to compute the effective address of the instruction, as required by the claim. And it is beyond one's reasonable imagination to see how the cited passage of the Guerra et al. reference teaches that element in any way whatsoever, much less in combination with the claim limitation that the computing step is executed responsive to the current effective address delay being less than zero. Furthermore, Appellants wish to note that this cited passage allegedly citing the "clock cycle calculation feature" has nothing whatsoever to do with the portion of the Guerra et al. reference applied against claim 1, which teaches the executing of a delay slot instruction following a conditional branch in response to receiving an interrupt. As such, Appellants submit that this passage of the Guerra et al. reference does not further describe the carrying out of the alleged calculating that is implicitly taught by the passage of the Guerra et al. reference that is applied against claim 1, and therefore cannot reasonably be applied against the further limitation, in claim 2, of the calculating step of claim 1.

Therefore, Appellants submit that the applied references fail to disclose or suggest the requirements of claim 2. As such, Appellants respectfully submit that the final rejection of claim 2 is necessarily based on the improper hindsight use of Appellants' own teachings.

For these reasons, Appellants respectfully submit that the final rejection of claim 2 is also in error, and request its reversal.

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[34] Guerra et al., *supra,* page 965, §2.2, ¶2.
[35] Office Action, *supra,* page 11.

For the foregoing reasons, therefore, Appellants respectfully submit that the final rejection under §103 of claims 1 and 2, as unpatentable over the combination of the Laurenti et al. and Guerra et al. references, is in error. Reversal of the final rejection of the claims in this case is therefore respectfully requested.

Respectfully submitted,

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Claims appendix:

1. A method for determining in software the effective address of instructions in a program executed on a pipelined architecture where there is no external visibility into the pipeline, the method comprising the steps of:

executing a first program;

determining that a first instruction is in the pipeline;

calculating the current effective address delay of the instruction in the pipeline;

determining whether a valid effective address for the instruction is available based on the current effective address delay of the instruction;

computing the effective address of the instruction responsive to determining that a valid effective address is not available; and

reporting the effective address of the instruction.

2. The method of Claim 1 wherein the step of calculating comprises subtracting the number of clock cycles that have occurred since the instruction entered the pipeline from the number of clock cycles required to compute the effective address of the instruction;

wherein the determining step comprises determining whether the current effective address delay is 0;

and wherein the step of computing is executed responsive to the current effective address delay being less than 0.

Evidence appendix:

None.

Related proceedings appendix:

None.